REMARKS

Pending Claims:

The status of the current claims are as follows:

Pending	1, 3-4, 6-7, 9, 11-13, 15-16, 20-26, 28-29, 31-32, 34, 36, 37, 39, 40, 42-43, 45, and 47-57
Unaltered since filing	4, 9, 28, 29, 34, 39, and 45
Amended by this Response	1, 3, 6, 7, 13, 26, 31-32, 37, 42 43, 47-50, and 57
Previously amended or added, but unchanged in this response	11-12, 15, 16, 20-25, 36, 47, and 51-56
Previously cancelled	2, 5, 8, 10, 14, 17-19, 27, 30, 33, 35, 38, 41, 44, and 46
Cancelled in this Response	40, 58

Entry of these amendments is respectfully requested.

Amendments to the Drawings and the Specification:

The drawings were objected to for failure to show the slave processor providing a clock signal to the synchronous random access memory. In response, the Applicant has amended Figure 1 by adding the clock signal 113, 123. This signal is supported by paragraph **0020** of the Specification:

> This method is needed for synchronous volatile memory since the processor during power-up does not supply the clock [113, 123] for about 10 execution cycles that is needed to read data from synchronous memory. The no-op command is a `filler` for this interval until the processor produces the clock [113, 123].

This language has been amended in this Response to refer to the new figure numbers 113, 123, as shown in brackets in the above quotation. The clock signal is also supported in the original specification at paragraph **0023:**

> Slave processing units may, however, be designed only to boot asynchronously from flash devices. Accordingly, the slave processing unit will not supply a synchronous clock output during its initial addressing of the memory devices. Another synchronous clock issue is the inability to change the slave processing unit's internal phase lock loop (PLL) to a different operation frequency while using the volatile memory boot architecture. It is sometimes common for a processor to start at a low clock frequency and to change the PLL to a much higher operating frequency during the bootstrap sequence. When this occurs, the synchronous clock stops momentarily and then restarts again but is erratic until a determined settling time occurs. By using the correct sequence of No-Operation instructions, as mentioned previously, and instruction cache, these processing units can

bootstrap from the synchronous SRAM devices where the SRAM clock is discontinuous through the bootstrap sequence.

All other changes to Figure 1 are minor changes to the text labels having no substantive effect.

Claim Objections--General:

The office action objected to claims 1 and 47 due to the inappropriate use of the definite article "the" in claim 1 and the lack of a space between the works "port" and "static" in claim 47. The above amendments correct these informalities.

Claim Rejections—35 USC § 112:

The office action has rejected claims 1, 3, 6, 7, 26, 31, 32, 37, 39, 42, 43, 50, and 51 under 35 USC § 112, second paragraph. In response, claims 1, 3, 6, 7 have been amended to clarify all references to the "processor" so as to explicit state either the first processor or the second processor. Claims 26, 31, and 32 have been amended so that all references to a processor or microprocessor refer to either a "master processor" or a "second processor."

Claims 37 and 43 have been amended to remove all references to the master processor. Claim 37 now refers only to the "processor" that utilizes the boot code stored in the volatile memory device. Claim 42 introduces "additional processors" which also utilize boot code stored in additional volatile memory devices. Claim 43 refers to the processor of claim 37 and the additional processors of claim 42 jointly as "processors." In this way, the ambiguities original found in claims 37, 39, 42, and 43 have been corrected.

Claim 50 has been correct to replace the reference to a "nonvolatile memory devices" with a reference to a "volatile memory devices" at line 4.

The Applicant appreciates the detailed review of the claims performed by the Examiner, and respectfully submits that the currently amended claims meet the requirements of Section 112, paragraph 2.

Rejection under 35 U.S.C. §103

The office action rejected many of the claims as obvious over Anderson (U.S. Patent No. 5,898,869) in view of Raatz (U.S. Patent No. 5,546,355), or in view of the

Anderson and Raatz further in view of Von Ahnen (U.S. Patent No. 6,400,717) or Ishinabe (U.S. Patent No. 5,572,468). These rejected claims included the original independent claims 1, 13, 26, and 37, 48, 49, and 57.

The Applicant gratefully notes that the Examiner found independent claims 50 and 52 to be patentable, and found dependent claim 58 patentable if written in independent format. The Applicant believes that all of the pending claims, as amended, are patentable over the prior art. The Applicants arguments can be divided into three primary thrusts, which are discussed separately below.

Synchronous Volatile Memory Provided a Processor

The present invention utilizes a synchrónous volatile memory to provide a bootstrap procedure to a processor. In the first office action dated January 25, 2005, the Examiner stated that the supplying of boot code to a processor through synchronous volatile memory was patentable over the then discovered prior art. Consequently, the applicant responded by placing this limitation into original independent claims 1, 26, and 37, and into the newly created independent claims 48, 49, 52, and 58. In this most recent office action, the Examiner rejects these claims as obvious. The Examiner acknowledges that none of the prior art references teaches the supplying of boot code through synchronous volatile memory. Rather, the Examiner uses Raatz for teaching that synchronous SRAM has advantages over asynchronous SRAM, including fewer external logic chips and higher system speeds. With this teaching from Raatz, the Examiner found it would be obvious to replace the asynchronous volatile memory chips of Anderson with the synchronous memory of Raatz.

The applicant notes that it is not possible to simply replace the synchronous memory of Raatz. As explained in the application in paragraph **0022**, when powering up a processor will not provide a usable clock signal for a number of execution cycles. When this clock signal provides the clock to the synchronous RAM, the memory will not be available to the processor and there will be a failure during boot-up. Nothing in Raatz, Anderson, or any of the cited prior art references addresses or even acknowledges this problem.

To remove any ambiguity regarding the claims, the Applicant has amended independent claims 1, 26, and 37 to explicitly recite that the slave or second processor provides the clock signal to the synchronous memory device during the boot process

and that the clock is allowed to stabilize after reset before beginning the boot process. Similarly, claim 48 specifically states that the slave processor provides "a clock signal to the synchronous static random access memory while booting with the slave bootstrap process stored on the synchronous static random access memory." These elements are not found in the prior art. In addition, because of the problems of reading from synchronous memory during the boot process, these elements cannot be found simply by combining the synchronous memory of Raatz with the apparatus of Anderson. Therefore, these claims, along with their related dependent claims, should be considered patentable over the prior art.

Pull-Down Resistor to Present No-Ops to the Booting Processor

The examiner has noted that claim 58 is patentable for the presence of "a pulldown resistor network on the data bus ensuring that the slave processor receives no-op instructions over the data bus during periods of clock instability." Claim 58 has now been cancelled, with the limitations of claim 58 being incorporated into claim 57. A similar limitation was placed in independent claim 49. Claims 49 and 57 should therefore now be considered patentable over the prior art.

Provision of Identity to Multiple Processors through Volatile Memory

The current office action states that claim 50 is patentable due to the presence of "a master processor storing identity in the volatile memories of a plurality of slave processors, each slave processor obtaining the identity from its own volatile memory." Newly amended dependent claim 7 and independent claim 13 have similar limitations, in which a master processor provides identity to each of a plurality of slave processors "by posting information through the volatile memory devices" used to store and deliver boot code for the slave processors. The office action rejected the original claims 7 and 13 by stating that Anderson teaches a first processor providing identity information to a plurality of processors by posting information through volatile memory at column 6, lines 16-25.

The Applicant respectfully disagrees with this understanding of Anderson. The recited section of Anderson discusses the fact that the START* control signal is responsive to an access by the host computer to a particular I/O address location. col. 6, lines 16-18. Each PCMCIA card can have a separate I/O address to trigger its processor

boot. col. 6, lines 20-25. This address is chosen by the "system configuration" and is implemented by the PCMCIA interface (17). col. 6, lines 18-20. The system configuration is itself stored in a non-volatile configuration memory EEPROM (15), which is connected directly to the PCMCIA interface (17). col. 4, lines 23-31; and Figures 1 and 2. Anderson further discusses the assignment of identities at col. 7, lines 40-62. This description further explains that identity information is stored in EEPROM (15) and is read by the PCMCIA interface (17), from which it is read and interpreted by host computer (11). Thus, all configuration information in Anderson is stored in a non-volatile EEPROM memory, and is used by the PCMCIA interface (17) to communicate with the host (11). The information is never stored in, or even present in, the volatile memory (39) that is used to boot the processor (31). Consequently, Anderson does not teach the placement of the identity information into the volatile memory used to boot the processor, as required by claims 7, 13, and 50. In addition, since the identity information is pre-programmed and stored in non-volatile EEPROM (15), the technique of Anderson does not allow the dynamic re-assignment of identities to processors that is allowed by the technique claimed in claims 7, 13, and 50. Consequently, these claims, and all related dependent claims, should be considered patentable over the prior art.

CONCLUSION

All of the claims remaining in this application should now be seen to be in condition for allowance. The prompt issuance of a notice to that effect is solicited.

Respectfully submitted,
COMPUTER NETWORK
TECHNOLOGY CORPORATION
By its attorneys:

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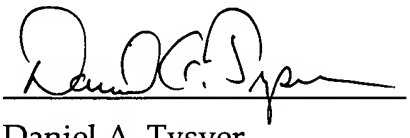

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